REMARKS

Claims 1-19 were examined and reported in the Office Action. Claims 1-19 are rejected. Claims 1, 11 and 17 are amended. Claims 1-19 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. §102(b) and §102(e)

A. It is asserted in the Office Action that claims 1-4, 6-15, and 17-18 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,966,544 issued to Sager ("Sager"). Applicant respectfully disagrees.

According to MPEP §2131, "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 1 contains the limitations of "a replay queue to receive a plurality of instructions; an execution unit to execute the plurality of instructions; a scheduler coupled between the replay queue and the execution unit to speculatively schedule instructions for execution based on data dependencies and expected latencies of said plurality of instructions; a checker coupled to the execution unit to determine whether each instruction of the plurality of instructions has executed successfully, and coupled to the replay queue to dispatch to the replay queue each instruction that has not executed successfully, and a counter to count a number of times an instruction has one of executed and replayed, wherein independent instructions and

associated dependent instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available."

Applicant's amended claim 11 contains the limitations of "[a] processor comprising: a replay queue to receive a plurality of instructions; at least two execution units to execute the plurality of instructions; at least two schedulers coupled between the replay queue and the execution units to schedule instructions for execution based on data dependencies and instruction latencies; a counter to count a number of times an instruction has one of executed and replayed, and a checker coupled to the execution units to determine whether each instruction has executed successfully, and coupled to the replay queue to communicate each instruction that has not executed successfully, wherein independent instructions and associated dependent instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available."

Applicant's amended claim 17 contains the limitations of "receiving an instruction of a plurality of instructions; placing the instruction in a queue with other instructions of the plurality of instructions; speculatively re-ordering those of the plurality of instructions in a scheduler based on data dependencies and instruction latencies; dispatching one of the plurality of instructions to an execution unit to be executed; executing the instruction; determining whether the instruction executed successfully; routing the instruction and all associated dependent instructions back to the queue if the instruction did not execute successfully; retiring the instruction if the instruction executed successfully and allowing the instruction's associated dependent instructions to execute, and counting a number of times an instruction has one of executed and replayed, wherein the instruction and associated dependent instructions are executed if the number of times the instruction has one of executed and replayed is less than a predetermined value and if the number of times the instruction has one of executed and

replayed exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available."

Therefore, Applicant's claimed invention provides a correct scheduling of dependent instructions for replay allowing for optimum performance and reduced latency.

Sager discloses a microprocessor having a replay architecture for data speculation in executing an instruction. Sager also discloses a checker for validating speculated executed instructions. Sager, however, does not teach, disclose or suggest Applicant's amended claim 1 limitations of "a scheduler coupled between the replay queue and the execution unit to speculatively schedule instructions for execution based on data dependencies and expected latencies of said plurality of instructions," or "a counter to count a number of times an instruction has one of executed and replayed, wherein independent instructions and associated dependent instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available." Also, Sager does not teach, disclose or suggest Applicant's amended claim 11 limitations of "at least two schedulers coupled between the replay queue and the execution units to schedule instructions for execution based on data dependencies and instruction latencies" or "independent instructions and associated dependent instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available." Further, Sager does not teach, disclose or suggest Applicant's amended claim 17 limitations of "speculatively re-ordering those of the plurality of instructions in a scheduler based on data dependencies and instruction latencies" or "the instruction and associated dependent instructions are executed if the number of times the instruction has one of executed and replayed is less than a predetermined value and if the number of times the instruction has one of executed and replayed exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available."

Therefore, since Sager does not disclose, teach or suggest all of Applicant's amended claims 1, 11 and 17 respective limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to Sager. Thus, Applicant's amended claims 1, 11 and 17 are not anticipated by Sager. Additionally, the claims that depend directly or indirectly on claims 1, 11 and 17, namely claims 2-4 and 6-10, 12-15, and 18, respectively, are also not anticipated by Sager for the above same reason.

Accordingly, withdrawal of the 35 U.S.C. §102(b) rejections for claims 1-4, 6-15, and 17-18 are respectfully requested.

B. It is asserted in the Office Action that claims 1-4, 6, 9-15, and 17-19 are rejected under 35 U.S.C. §102(e) as being anticipated by U. S. Patent No. 6, 212,626 issued to Merchant et al. ("Merchant"). Applicant respectfully disagrees.

Applicant's amended claims 1, 11 and 17 are listed above.

Merchant is a continuation-in-part of Sager, which is discussed above in section I(A). Merchant discloses a checker that includes a scoreboard for receiving an external replay signal, and logic for determining whether an instruction executed correctly based on the scoreboard and external replay signal. Merchant, however, does not teach, disclose or suggest Applicant's amended claim 1 limitations of "a scheduler coupled between the replay queue and the execution unit to speculatively schedule instructions for execution based on data dependencies and expected latencies of said plurality of instructions," or "a counter to count a number of times an instruction has one of executed and replayed, wherein independent instructions and associated dependent instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available." Also, Merchant does not teach, disclose or suggest Applicant's amended claim 11 limitations of "at least two schedulers coupled between the replay queue and the execution units to schedule instructions for execution based on data dependencies and instruction latencies" or "independent

instructions and associated dependent instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available." Further, Merchant does not teach, disclose or suggest Applicant's amended claim 17 limitations of "speculatively re-ordering those of the plurality of instructions in a scheduler based on data dependencies and instruction latencies" or "the instruction and associated dependent instructions are executed if the number of times the instruction has one of executed and replayed is less than a predetermined value and if the number of times the instruction has one of executed and replayed exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available."

Therefore, since Merchant does not disclose, teach or suggest all of Applicant's amended claims 1, 11 and 17 respective limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Merchant. Thus, Applicant's amended claims 1, 11 and 17 are not anticipated by Merchant. Additionally, the claims that depend directly or indirectly on claims 1, 11 and 17, namely claims 2-4, 6 and 9-10, 12-15, and 18-19, respectively, are also not anticipated by Merchant for the above same reason.

Accordingly, withdrawal of the 35 U.S.C. §102(e) rejections for claims 1-4, 6, 9-15, and 17-19 are respectfully requested.

II. 35 U.S.C. §103(a)

Claims 5, 16, and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sager, as applied above in view of U. S. Patent No. 5,944,818 issued to Baxter et al., ("Baxter"). Applicant respectfully disagrees.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary

skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's claims 5, 16 and 19 depend on amended claims 1, 11 and 17, respectively. Applicant has discussed amended claims 1, 11 and 17 above with regard to Sager.

Baxter discloses a device and technique for accelerating instruction restart. Baxter further discloses determining when a restart condition exists and delivering the macro-instruction to a decode unit when the restart condition is indicated. Baxter, however, does not teach, disclose or suggest "Applicant's amended claim 1 limitations of "a scheduler coupled between the replay queue and the execution unit to speculatively schedule instructions for execution based on data dependencies and expected latencies of said plurality of instructions," or "a counter to count a number of times an instruction has one of executed and replayed, wherein independent instructions and associated dependent instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available." Also, Baxter does not teach, disclose or suggest Applicant's amended claim 11 limitations of "at least two schedulers coupled between the replay queue and the execution units to schedule instructions for execution based on data dependencies and instruction latencies" or "independent instructions and associated dependent

instructions are executed if the counter is less than a predetermined value and if the counter exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available." Further, Baxter does not teach, disclose or suggest Applicant's amended claim 17 limitations of "speculatively re-ordering those of the plurality of instructions in a scheduler based on data dependencies and instruction latencies" or "the instruction and associated dependent instructions are executed if the number of times the instruction has one of executed and replayed is less than a predetermined value and if the number of times the instruction has one of executed and replayed exceeds the predetermined value the instruction is prevented from executing until data required by the instruction is available."

Therefore, even if the disclosures of Sager and Baxter were combined the resulting invention would still not include all the limitations of amended claims 1, 11 and 17 as neither Sager, Baxter, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's amended claims 1, 11 and 17, as listed above. Since neither Sager, Baxter, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claims 1, 11 and 17, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claims 1, 11 and 17 are not obvious over Sager in view of Baxter since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1, 11 and 17, namely claims 5, 16, and 19, respectively, would also not be obvious over Sager in view of Baxter for the same reason.

Accordingly, withdrawal of the 35 U.S.C. §103(a) rejection for claims 5, 16, and 19 are respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-19 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: April 20, 2004

By: _____
Steven Laut, Reg. No. 47,736

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on April 20, 2004.

Nadya Gordon April 20, 2004